A H

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,104	02/07/2001	Yuuichi Hirano	202887US2	4460

22850 7590 05/16/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 05/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/778,104	HIRANO ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *3,4 and 7-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The Applicant argues that the reason's for obviousness in the 35 U.S.C. 103(a) rejection over Applicant's Admitted Prior Art in view of U.S. Patent No: 5,266,825 Tsukada et al. is not properly motivated. The examiner has considered Applicant's arguments and finds them to be non-persuasive because Tsukada et al. explicitly states reasons for creating offset regions in the source and drain. Tsukada et al. teaches that by decreasing the gate insulator thickness makes it possible to reduce the channel width, which in return the overlapping area decreases between the source or drain from the gate resulting in higher probability of defects due to shorts, (Tsukada et al. Col. 7 Lines 37-43). Tsukada et al.'s novel invention is creating the offset regions in the source and drain to reduce the chances of these defects from shorts from occurring, (Tsukada et al. Col. 3 Lines 1-11). The functions of Tsukada et al.'s novelty maybe different from the Applicant's, but does not make the matter patentable as stated in 35 U.S.C. 103(a). The 35 U.S.C. 103(a) rejection will stand as is.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art in view of U.S. Patent No. 5,266,825 Tsukada et al.

2. Referring to claim 1, a semiconductor device comprising: an SOI substrate, (Applivant's Admitted Prior Art Figure 29 #105), having a semiconductor substrate, (Applicant's Admitted Prior Art Figure 29 #106), a dielectric layer, (Applicant's Admitted Prior Art Figure 29 #107), and a semiconductor layer, (Applicant's Admitted Prior Art Figure 29 #108), formed in this order; a transistor having a drain region, (Applicant's Admitted Prior Art Figure 29 #104), and a source region, (Applicant's Admitted Prior Art Figure 29 #104), respectively formed in said semiconductor layer, (Applicant's Admitted Prior Art Figure 29 #108), and a gate electrode, (Applicant's Admitted Prior Art Figure 29 #101), formed via a gate dielectric film, (Applicant's Admitted Prior Art Figure 29 #113), on a channel region, (Applicant's Admitted Prior Art Figure 29 #110), sandwiched between said drain region, (Applicant's Admitted Prior Art Figure 29 #104), and said source region, (Applicant's Admitted Prior Art Figure 29 #104); an interlayer dielectric film, (Applicant's Admitted Prior Art Figure 29 #118), formed on said transistor; a drain wiring, (Applicant's Admitted Prior Art Figure 29 #119), and a source wiring, (Applicant's Admitted Prior Art Figure 29 #119), formed on said interlayer dielectric film, (Applicant's Admitted Prior Art Figure 29 #118); a first conductor, (Applicant's Admitted Prior Art Figure 29 #117), formed in said interlayer dielectric film, (Applicant's Admitted Prior Art Figure 29 #118), for connecting said drain wiring, (Applicant's Admitted Prior Art Figure 29 #119), to said drain region, (Applicant's Admitted Prior Art Figure 29 #104); and a second conductor, (Applicant's Admitted Prior Art Figure 29 #117), formed in said interlayer dielectric film, (Applicant's Admitted Prior Art Figure 29 #118), for connecting said source wiring, (Applicant's Admitted Prior Art Figure 29 #119), to said source region, (Applicant's Admitted Prior Art Figure 29 #104), wherein said drain region, (Applicant's Admitted Prior Art Figure 29 #104 and Tsukada

et al. Figure 1a #9), has a first part, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #9), being adjacent to said channel region and, (Applicant's Admitted Prior Art Figure 29 #110 and Tsukada et al. Figure 1a in the area of #4), and a second part, (Tsukada et al. Figure 1a #9b), formed to protrude from said first part, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #9), so that a part of outer peripheries of said drain region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #9), extends away from said gate electrode, (Applicant's Admitted Prior Art Figure 28 #101 and Tsukada et al. Figure 1a #2), in a plan view, and said first conductor, (Applicant's Admitted Prior Art Figure 29 #117 and Tsukada et al. Figure 1a #11), is connected to said second part, (Tsukada et al. Figure 1a #9b), of said drain region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #9).

The Applicant's Admitted Prior Art teaches all of the claimed matter in claim 1 except for the drain region having a second part that protrudes away from the first part and is connected to the drain conductor, but Tsukada et al. does. It would have been obvious to combine the teachings of the Applicant's Admitted prior Art with Tsukada et al. because it is well known to one skilled in the art that increasing the effective mobility of the transistor will in effect increase defects due to shorts between the gate and the source and/or drain and an offset region in the source or drain region would increase the area between the source/drain and the gate, which would decrease the chances of shorts or parasitic capacitances, (Tsukada et al. Col. 3 Lines 4-11).

3. Referring to claim 2, a semiconductor device, wherein said first part of said drain region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #9), has a width of 0.2 to 0.5 μm with respect to a channel length direction of said channel region, (Applicant's

Admitted Prior Art Figure 29 #110 and Tsukada et al. Figure 1a in the area of #4), and said second part of said drain region, (Tsukada et al. Figure 1a #9b), has a length of 0.1 to 0.5 μm with respect to a direction protruding from said first part of said drain region.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. Referring to claim 5, a semiconductor device, wherein said source region has a first part, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #8), being adjacent to said channel region, (Applicant's Admitted Prior Art Figure 29 #110 and Tsukada et al. Figure 1a in the area of #4), and a second part, (Tsukada et al. Figure 1a #8b), formed to protrude from said first part, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #8), so that a part of outer peripheries of said source region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #8), extends away from said gate electrode, (Applicant's Admitted Prior Art Figure 28 #101 and Tsukada et al. Figure 1a #2), in a plan view, and said second conductor, (Applicant's Admitted Prior Art Figure 29 #117 and Tsukada et al. Figure 1a #11), is connected to said second part of said source region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #8b).

The Applicant's Admitted Prior Art teaches all of the claimed matter in claim 1 except for the source region having a second part that protrudes away from the first part and is connected to the source conductor, but Tsukada et al. does. It would have been obvious to combine the teachings of the Applicant's Admitted prior Art with Tsukada et al. because it is well known to one skilled in the art that increasing the effective mobility of the transistor will in effect increase defects due

to shorts between the gate and the source and/or drain and an offset region in the source or drain region would increase the area between the source/drain and the gate, which would decrease the chances of shorts or parasitic capacitances, (Tsukada et al. Col. 3 Lines 4-11).

5. Referring to claim 6, a semiconductor device, wherein said first part of said source region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #8), has a width of 0.2 to 0.5 μm with respect to a channel length direction of said channel region, (Applicant's Admitted Prior Art Figure 29 #110 and Tsukada et al. Figure 1a in the area of #4), and said second part of said source region, (Tsukada et al. Figure 1a #8b), has a length of 0.1 to 0.5 μm with respect to a direction protruding from said first part of said source region, (Applicant's Admitted Prior Art Figure 28 #104 and Tsukada et al. Figure 1a #8).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
May 13, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800